

SPECIFICATION

Graphic Type STN Dot Matrix LCD Module

JM12864A

SHENZHEN JINGHUA DISPLAYS CO.,LTD.

● GENERAL SPECIFICATION

128 X 64 dots display

SAM SUNG LCD driver:KS0107B and KS0108B

Interface with 8-bit MPU (directly connected to M6800 serial MPU)

Display Specification

Display dot: 128 X 64

Display type: STN and FSTN

Display color-Display background color: Black-Yellow Green,Blue-Gray, Black-White

Polarizer mode: Positive,Negative;Reflective ,Transflective,Transmissive

Viewing angle: 6:00 and 12:00

Display duty: 1/64

Driving bias: 1/9

Display RAM: 8192 bits

Mechanical characteristics (Unit:mm)

External dimension: 78.0 X 70.0 X 10.0 (13.0 for Side LED Backlight;
15.0 for Bottom LED Backlight)

View area: 62.0 X 44.0

Dot size: 0.39 X 0.55

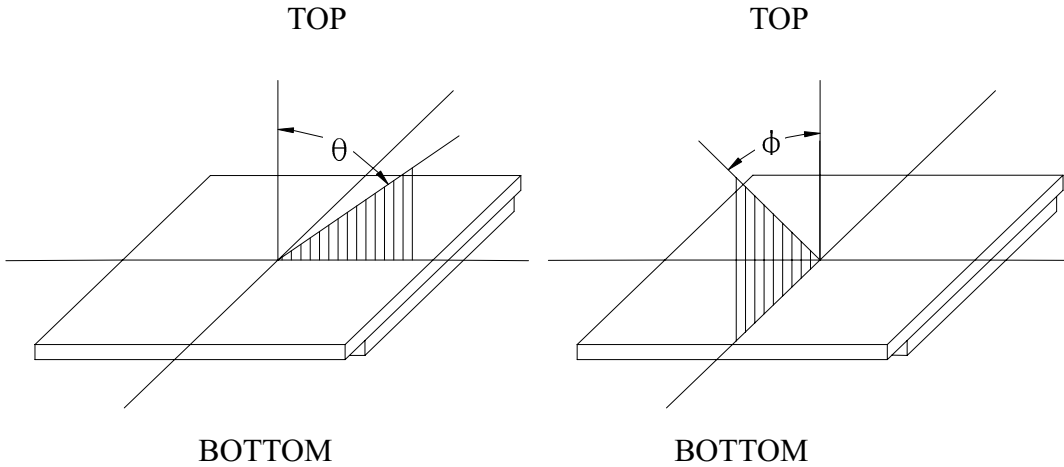
Dot pitch: 0.44 X 0.60

Weight: 56g (75g for Side LED backlight;82g for Bottom LED Backlight)

POWER: negative power, +5V

● **Optical Characteristics**

(1) Definition of viewing Angle



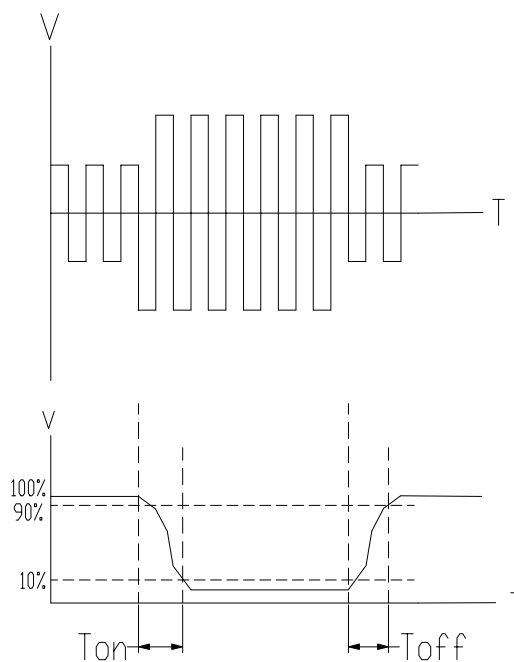
(2) Definition of Contrast Ratio:

$$\text{Contrast Ratio} = \frac{\text{Reflectance value of non-selected state brightness}}{\text{Reflectance value of selected state brightness}}$$

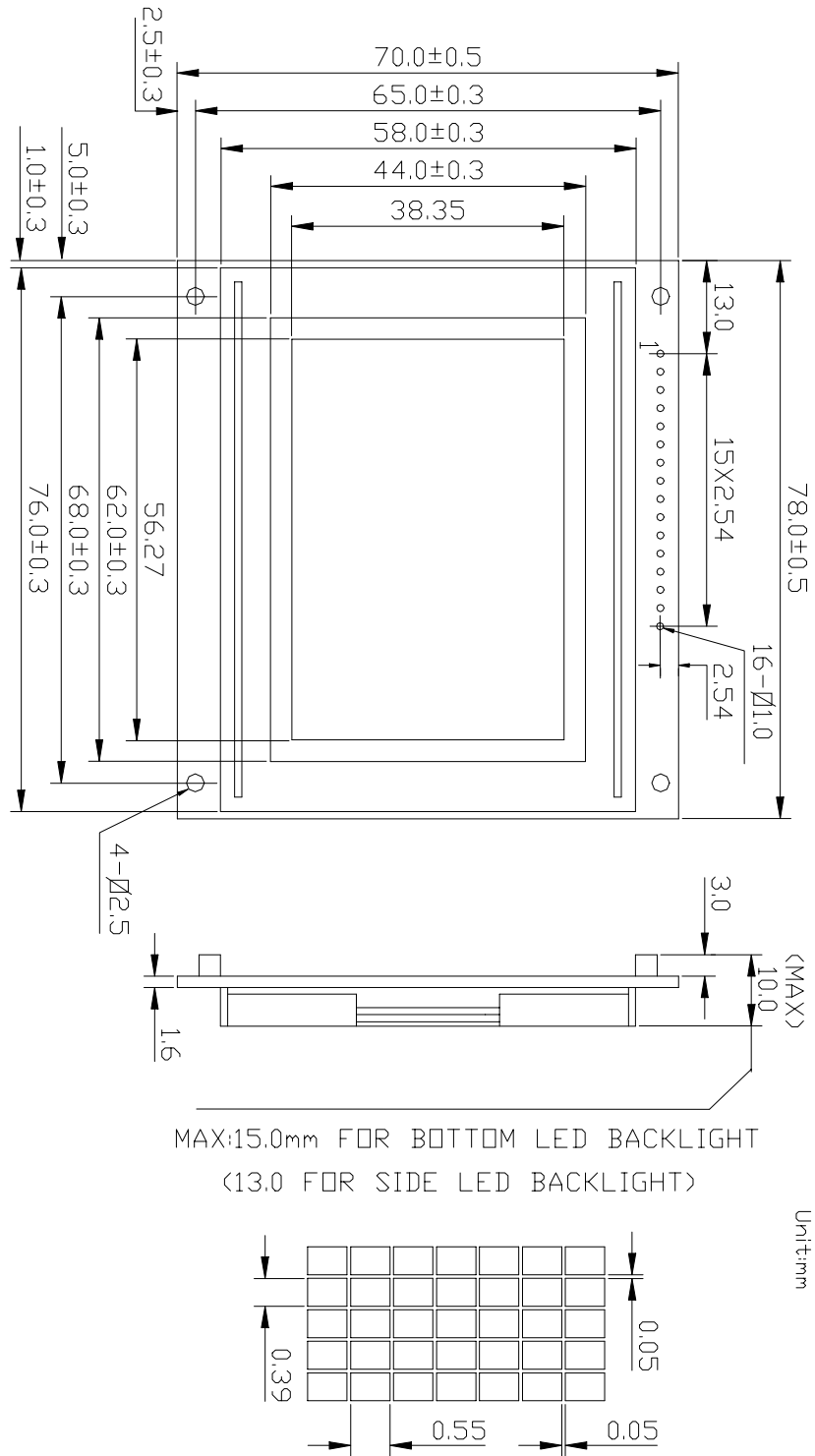
Test condition : standard A light source

(3) Response Time

Response time is measured as the shortest period of time possible between the change in state of an LCD segment as demonstrated below



● External Dimension



● **Absolute Maximum Ratings For Side LED Backlight**

Parameter	Symbol	Test condition	Min	Type	Max	Unit
LED Forward Consumption Current	I_f	Ta=25°C Vf=4.1V	-	83	-	mA
LED Allowable Dissipation	P_d		-	350	-	mW

● **Absolute Maximum Ratings For Bottom LED Backlight**

Parameter	Symbol	Test condition	Min	Type	Max	Unit
LED Forward Consumption Current	I_f	Ta=25°C Vf=4.1 V	-	192	-	mA
LED Allowable Dissipation	P_d		-	790	-	mW

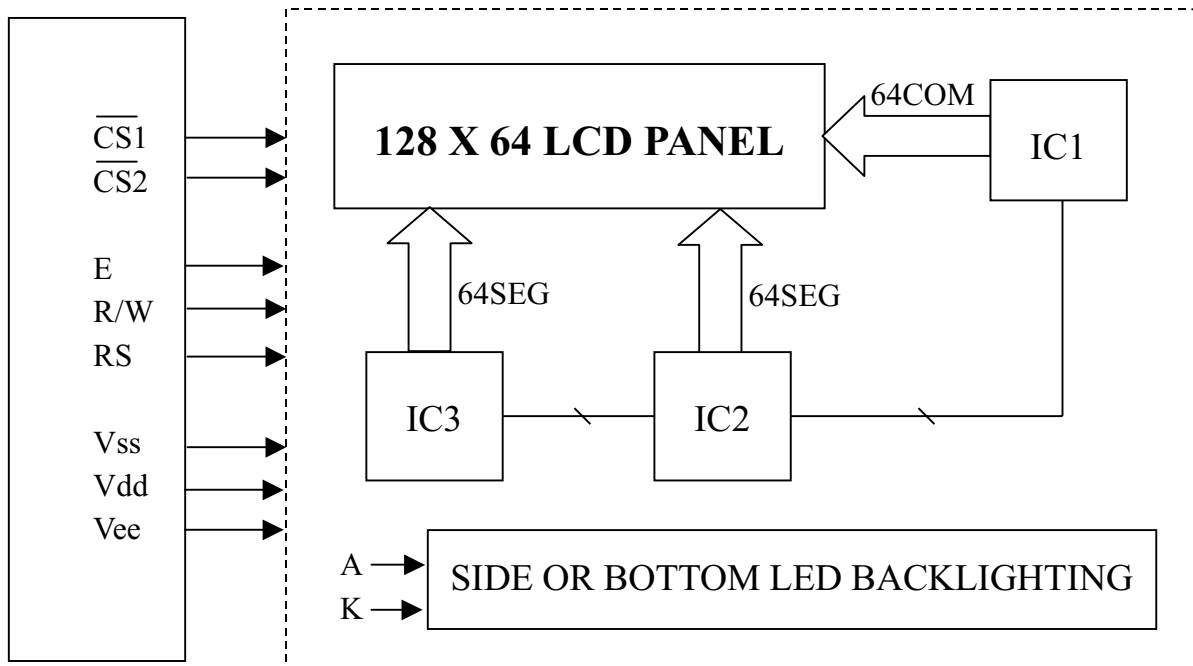
● **Absolute Maximum Ratings**

Item	Symbol	Condition	Standard Value		Unit
			Min	Max	
Supply Voltage for logic	Vdd	Ta=25°C	-0.3	7.0	V
Supply Voltage for LCD	Vee		Vdd-19.0	Vdd+0.3	V
Input Voltage	Vi		-0.3	Vdd+0.3	V
Operating Temp(T)	Top	-	0	50	°C
Storage Temp(T)	Tstg	-	-20	70	°C
Operating Temp(HT)	HTop	-	-20	70	°C
Storage Temp(HT)	HTstg	-	-30	80	°C
Operating Temp(EHT)	EHTop	-	-30	80	°C
Storage Temp(EHT)	EHTstg	-	-40	80	°C

● **Electrical Characteristics** (Ta=25°C, Vdd= 5.0V)

Item	Symbol	Condition	Standard Value			Unit
			Min	Type	Max	
Supply Voltage for logic	Vdd-Vss	-	4.5	5.0	5.5	V
Supply Current for logic	Idd	Vdd=5.0	-	4.0	-	mA
Driving Current for LCD	Iee	Vee=-7.8	-	2.8	-	mA
Driving Voltage for LCD	Vdd-Vee	25°C	-	12.8	-	V
Input Voltage“H” level	V _{IH}	H	0.7Vdd	-	Vdd	V
Input Voltage “L” level	V _{IL}	L	0	-	0.8	V

● **Block Diagram**

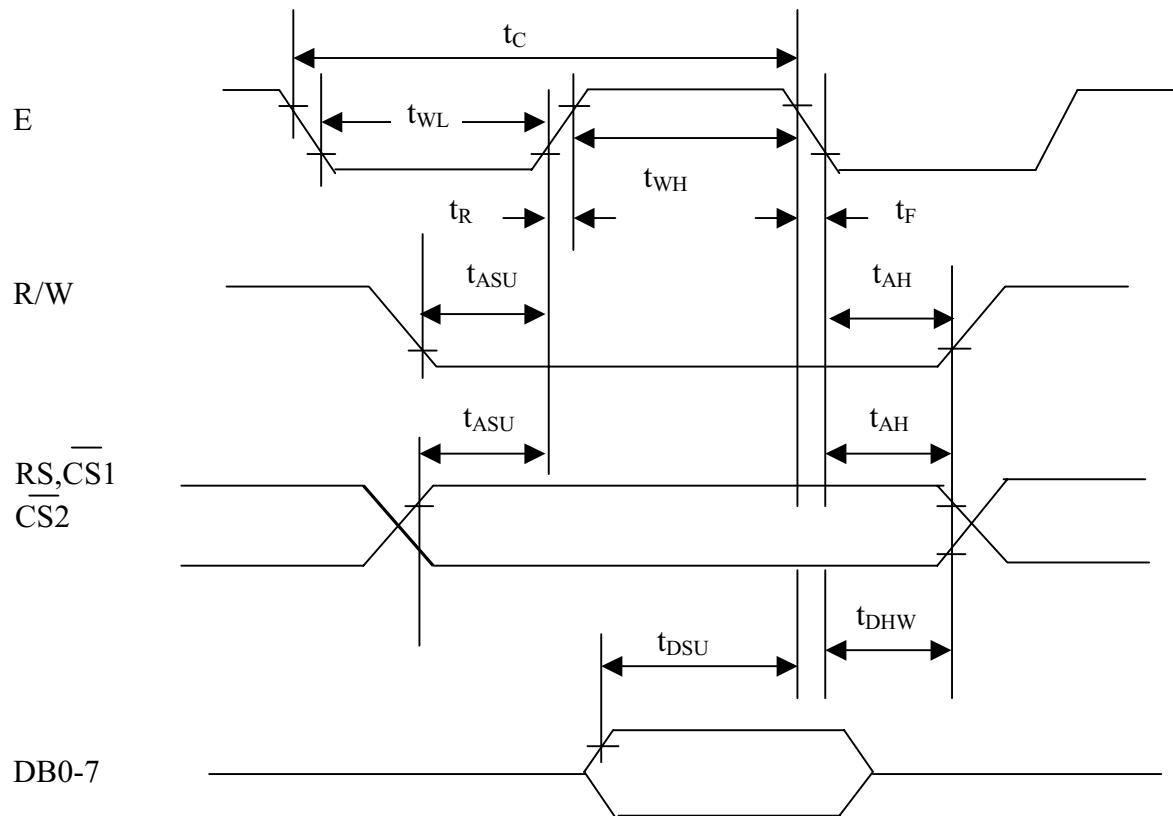


● Pin assignment

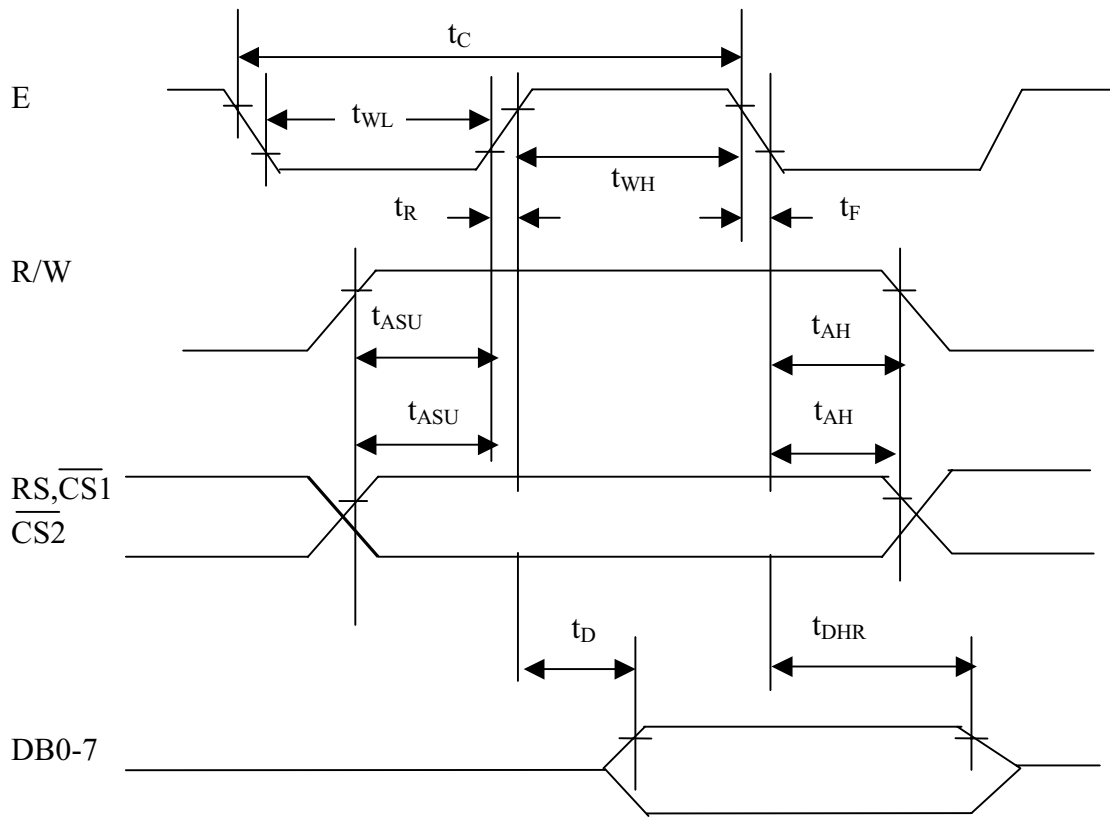
Pin NO.	Symbol	Function		Remark
1	$\overline{\text{CS1}}$	Chip Select Signal For IC3 When L		
2	$\overline{\text{CS2}}$	Chip Select Signal For IC2 When L		
3	Vss	Power Supply	0V	
4	Vdd		+5V	
5	Vee		For LCD	Variable
6	RS	Register Select (H:Data L:Instruction)		
7	R/W	L:MPU to LCM H:LCM to MPU		
8	E	Enable		
9	DB0	Data Bit 0		
10	DB1	Data Bit 1		
11	DB2	Data Bit 2		
12	DB3	Data Bit 3		
13	DB4	Data Bit 4		
14	DB5	Data Bit 5		
15	DB6	Data Bit 6		
16	DB7	Data Bit 7		
	A	Anode of LED Unit		
	K	Cathode of LED Unit		

● MPU Interface

Characteristic	Symbol	Min	Typ	Max	Unit
E Cycle	t_c	1000	-	-	ns
E High Level Width	t_{WH}	450	-	-	ns
E Low Level Width	t_{WL}	450	-	-	ns
E Rise Time	t_R	-	-	25	ns
E Fall Time	t_F	-	-	25	ns
Address Set-Up Time	t_{ASU}	140	-	-	ns
Address Hold Time	t_{AH}	10	-	-	ns
Data Set-Up Time	t_{DSU}	200	-	-	ns
Data Delay Time	t_D	-	-	320	ns
Data Hold Time(Write)	t_{DHW}	10	-	-	ns
Data Hold Time(Read)	t_{DHR}	20	-	-	ns

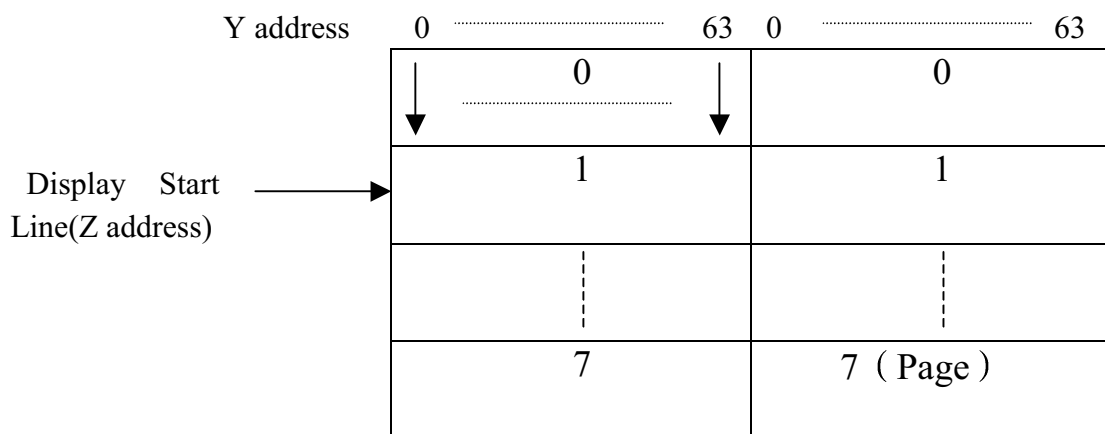


MPU writing timing



MPU read timing

● Reflector of Screen and Display RAM



Correspondence with data bits and arrow direction



● DISPLAY CONTROL INSTRUCTION

Instruction	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Function	
Display ON/OFF	L	L	L	L	H	H	H	H	H	L/H	Controls the display on or off. Internal status and display RAM data is not affected. L:OFF, H:ON	
Set address (Y address)	L	L	L	H	Y address (0~63)						Sets the Y address in the Y address counter.	
Set Page (X address)	L	L	H	L	H	H	H	Page (0~7)			Sets the X address at the X address register.	
Display Start Line (Z address)	L	L	H	H	Display start line (0~63)						Indicates the display data RAM displayed at the top of the screen.	
Status Read	L	H	B U S Y	L	O N / O F F	R E S E T	L	L	L	L	BUSY L:Ready H:In operation ON/OFF L:Display ON H:Display OFF RESET L:Normal H:Reset	
Write Display Data	H	L	Write Data									Writes data (DB0:7) into display data RAM,After writing instruction,Y address is increased by 1 automatically.
Read Display Data	H	H	Read Data									Reads data (DB0:7) from display data RAM to the data bus.

1.Display On/Off

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	1	1	1	D

The display data appears when D is 1 and disappears when D is 0.

Though the data is not on the screen with D=0, it remains in the display data RAM.

Therefore, you can make it appear by changing D=0 into D=1.

2.Set Address(Y Address)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0

Y address (AC0-AC5) of the display data RAM is set in the Y address counter.

An address is set by instruction and increased by 1 automatically by read or write operations of display data.

3.Set Page(X Address)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	1	1	AC2	AC1	AC0

X address (AC0-AC2) of the display data RAM is set in the X address register.

Writing or reading to or from MPU is executed in this specified page until the next page is set.

4.Display Start Line(Z Address)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	AC5	AC4	AC3	AC2	AC1	AC0

Z address (AC0-AC5) of the display data RAM is set in the display start line register and displayed at the top of the screen.

When the display duty cycle is 1/64 or others(1/32-1/64), the data of total line number of LCD screen, from the line specified by display start line instruction, is displayed.

5.Status Read

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	BUSY	0	ON/OFF	RESET	0	0	0	0

- **BUSY**
 When BUSY is 1,the Chip is executing internal operation and no instructions are accepted.
 When BUSY is 0,the Chip is ready to accept any instructions.

- **ON/OFF**
 When ON/OFF is 1,the display is on.
 When ON/OFF is 0,the display is off.

- **RESET**
 When RESET is 1,the system is being initialized.
 In this condition, no instructions except status read can be accepted.
 When RESET is 0,initializing has finished and the system is in the usual operation condition.

6.Write Display Data

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	D7	D6	D5	D4	D3	D2	D1	D0

Writes data (D0-D7) into the display data RAM.
 After writing instruction, Y address is increased by 1 automatically.

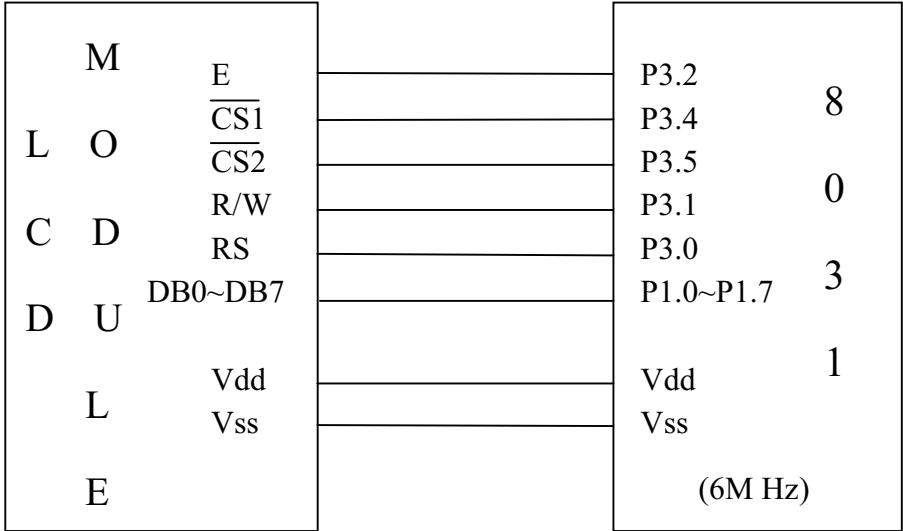
7.Read Display Data

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	D7	D6	D5	D4	D3	D2	D1	D0

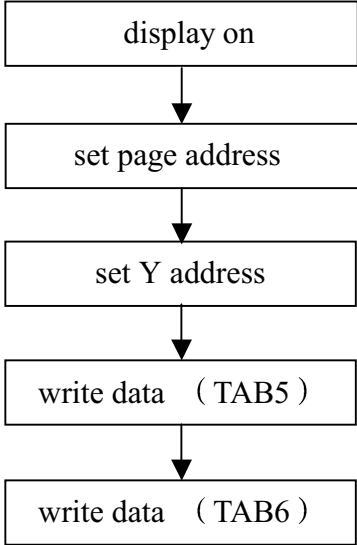
Reads data (D0-D7) from the display data RAM.
 After reading instruction, Y address is increased by 1 automatically.

● APPLICATION EXAMPLE

Application Circuit



Application Flowchart



Program Example

```

;***** THIS IS A 51 PROGRAM (128*64) *****
;  1    2    3    4    5    6    7    8    9--16
; CS1  CS2  Vss  Vdd  Vee  RS  R/W  E    DB0--DB7
; P3.4 P3.5                                P3.0 P3.1 P3.2  P1
;*****
        RS    EQU  P3.0
        R/W   EQU  P3.1
        E     EQU  P3.2
        CS1   EQU  P3.4
        CS2   EQU  P3.5
;*****
ORG     0000H
RESET:  MOV   R7, #04H
        LCALL DELAYXMS
        CLR  E
        SETB RS
        SETB CS1
        CLR  CS2
        CLR  RS
        MOV  P1, #3FH ;DISPLAY ON
        LCALL WRITE
        MOV  R7, #01H
        SETB CS2
        CLR  CS1
        CLR  RS
        MOV  P1, #3FH ;DISPLAY ON
        LCALL WRITE

MAIN:
        MOV  R7, #0FH
        MOV  DPTR, #TAB5
        LCALL ZXL
        MOV  R7,#0FH
        LCALL DELAYXMS
        MOV  DPTR,#TAB6
        LCALL ZXL
        MOV  R7,#0FH
        LCALL DELAYXMS

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LJMP MAIN

ZXL:

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CLR    CS1
SETB   CS2
LCALL  PAGE
LCALL  COM
CLR    CS2
SETB   CS1
LCALL  PAGE
LCALL  COM
RET

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ZXL0:  CLR    E
        CLR    CS1
        SETB   CS2
        CLR    RS
        SETB   R/W
        SETB   E
        MOV   A,  P1
        LCALL  PAGE
        LCALL  COM0
        CLR    CS2
        SETB   CS1
        LCALL  PAGE
        LCALL  COM0
        CLR    CS1
        CLR    RS
        MOV   P1, #3FH
        LCALL  WRITE
        RET

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PAGE:  CLR    E
        CLR    RS
        MOV   P1, #0C0H
        LCALL  WRITE
        MOV   P1, #40H
        LCALL  WRITE
        MOV   R0, #08H

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        MOV  R2, #0B8H
        MOV  P1, #0B8H
        LCALL WRITE
        RET
;*****
COM:   MOV  R1, #40H
        SETB RS
J4:    CLR  A
        MOVC A,  @A+DPTR
        MOV  P1,  A
        LCALL WRITE
        INC  DPTR
        DJNZ R1, J4
        CLR  RS
        INC  R2
        MOV  P1, R2
        LCALL WRITE
        MOV  P1, #40H
        LCALL WRITE
        DJNZ R0, COM
        RET
;*****
;      CPL
;*****
COM0:  MOV  R1, #41H
J40:   DEC  R1
        CLR  A
        ORL  A,  R1
        JZ   J50
        SETB RS
        CLR  A
        MOVC A,  @A+DPTR
        CPL  A
        MOV  P1,  A
        LCALL WRITE
        INC  DPTR
        SJMP J40
J50:   DEC  R0
        CLR  A

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    ORL A, R0
    JZ J60
    CLR RS
    INC R2
    MOV P1, R2
    LCALL WRITE
    MOV P1, #40H
    LCALL WRITE
    SJMP COM0
J60: RET
;*****
WRITE:
    CLR R/W
    CLR E
    SETB E
    LCALL DELAY2MS
    CLR E
    RET
;*****
DELAY2MS: MOV R6, #02H
          DELAY0: MOV R5, #0FH
          DELAY1: DJNZ R5, DELAY1
                  DJNZ R6, DELAY0
                  RET
;*****
DELAYXMS: MOV R5, #40H
          D1: MOV R6, #0FFH
          D2: DJNZ R6, D2
                  DJNZ R5, D1
                  DJNZ R7, DELAYXMS
                  RET
TAB5: DB 55H,0AAH,55H,0AAH,55H,0AAH,55H,0AAH
      DB 55H,0AAH,55H,0AAH,55H,0AAH,55H,0AAH
      DB 55H,0AAH,55H,0AAH,55H,0AAH,55H,0AAH
      DB 55H,0AAH,55H,0AAH,55H,0AAH,55H,0AAH
      DB 55H,0AAH,55H,0AAH,55H,0AAH,55H,0AAH
      DB 55H,0AAH,55H,0AAH,55H,0AAH,55H,0AAH
      DB 55H,0AAH,55H,0AAH,55H,0AAH,55H,0AAH
      DB 55H,0AAH,55H,0AAH,55H,0AAH,55H,0AAH

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DB 55H,0AAH,55H,0AAH,55H,0AAH,55H,0AAH

DB 55H,0AAH,55H,0AAH,55H,0AAH,55H,0AAH

DB 55H,0AAH,55H,0AAH,55H,0AAH,55H,0AAH

TAB6: DB 00H,00H,00H,00H,00H,00H,00H,00H

DB 00H,00H,00H,00H,00H,00H,00H,00H

DB 00H,00H,00H,00H,00H,00H,00H,00H

DB 00H,00H,00H,00H,00H,00H,00H,00H

DB 00H,00H,00H,00H,00H,00H,00H,00H

DB 00H,00H,00H,00H,00H,00H,00H,00H

DB 00H,00H,00H,00H,00H,00H,00H,00H

DB 00H,00H,00H,00H,00H,00H,00H,00H

DB 00H,00H,00H,00H,00H

DB 08H,18H,78H,70H,00H,00H,0E0H,78H

DB 10H,10H,90H,10H,10H,10H,90H,10H

DB 10H,10H,0D0H,78H,30H,20H,00H,00H

DB 00H,00H,00H,00H,00H,00H,00H,00H

DB 00H,00H,0F8H,0F0H,20H,00H,00H,00H

DB 00H,00H,0F8H,0F0H,20H,00H,0E0H,0C0H

DB 80H,00H,00H,00H,0F8H,0F0H,20H,00H,00H,00H,00H

DB 00H,00H,01H,02H,0EH

DB 1CH,08H,00H,00H,00H,0C0H,0A0H,98H

DB 8CH,87H,83H,81H,0F8H,0F0H,0A0H,81H

DB 83H,86H,8EH,9CH,0C0H,80H,00H,00H

DB 00H,00H,00H,00H,00H,00H,00H,08H

DB 08H,08H,0FFH,0FFH,08H,08H,0CH,0EH

DB 08H,00H,0FFH,0FFH,00H,00H,0FFH,0FFH

DB 00H,00H,00H,00H,0FFH,0FFH,00H,00H,00H,00H,00H,00H

DB 00H,00H,04H,04H,04H

DB 0FCH,0FEH,01H,00H,00H,80H,0C0H,60H

DB 30H,1CH,0FH,03H,0FFH,0FFH,03H,1CH

DB 38H,60H,0E0H,0C0H,80H,80H,00H,00H

DB 00H,00H,00H,00H,00H,20H,60H

DB 60H,30H,3FH,1FH,18H,08H,08H,84H

DB 60H,38H,1FH,07H,00H,00H,0FFH,7FH

DB 00H,00H,00H,00H,0FFH,0FFH,00H,00H,00H,00H,00H

DB 00H,00H,00H,00H,00H,01H
DB 03H,07H,00H,01H,01H,00H,00H,00H
DB 00H,00H,00H,00H,0FH,07H,00H,00H
DB 00H,00H,00H,01H,01H,01H,01H,00H
DB 00H,00H,00H,00H,00H,00H,00H
DB 00H,00H,00H,04H,04H,02H,01H,00H
DB 00H,00H,00H,00H,00H,00H,00H,00H
DB 00H,00H,00H,00H,0FH,07H,00H,00H,00H,00H

DB 00H,00H,00H,00H,00H
DB 00H,00H,00H,00H,00H,00H,00H,00H
DB 00H,00H,00H,00H,00H,00H,00H,00H
DB 00H,00H,00H,00H,00H,00H,00H,00H
DB 00H,00H,00H,00H,00H,00H,00H,00H
DB 00H,00H,00H,00H,00H,00H,00H,00H
DB 00H,00H,00H,00H,00H,00H,00H,00H
DB 00H,00H,00H,00H,00H,00H,00H,00H,00H,00H

DB 00H,00H,00H,00H,00H,00H
DB 00H,00H,00H,00H,00H,00H,00H,66H
DB 89H,89H,92H,67H,00H,00H,0FFH,10H
DB 10H,0FFH,00H,00H,0FFH,89H,9DH,81H
DB 0E3H,00H,0FFH,02H,1CH,20H,0FFH,00H
DB 0C7H,0A1H,91H,8DH,83H,0E1H,00H,0FFH
DB 08H,08H,0FFH,00H,00H,0FFH,89H,9DH,81H,0E3H
DB 00H,0FFH,02H,1CH,20H,0FFH,00H,00H

DB 00H,00H,00H,00H,00H
DB 00H,00H,00H,00H,00H,00H,00H,00H
DB 00H,00H,00H,00H,00H,00H,00H,00H
DB 00H,00H,00H,00H,00H,00H,00H,00H
DB 00H,00H,00H,00H,00H,00H,00H,00H
DB 00H,00H,00H,00H,00H,00H,00H,00H
DB 00H,00H,00H,00H,00H,00H,00H,00H
DB 00H,00H,00H,00H,00H,00H,00H,00H,00H,00H
DB 00H,00H,00H,00H,00H,00H,00H,00H
DB 00H,00H,00H,00H,00H,00H,00H,00H
DB 00H,00H,00H,00H,00H,00H,00H,00H
DB 00H,00H,00H,00H,00H,00H,00H,00H

DB 00H,00H,00H,00H,00H,00H,00H,00H
DB 00H,00H,00H,00H,00H,00H,00H,00H
DB 00H,00H,00H,00H,00H,00H,00H,00H
DB 00H,00H,00H,00H,00H,00H,00H,00H

DB 00H,00H,00H,00H,00H
DB 00H,00H,00H,00H,0F8H,0F0H,10H,10H
DB 10H,10H,10H,10H,10H,10H,0F0H,0F8H
DB 10H,00H,00H,00H,00H,00H,00H,00H
DB 00H,00H,00H,00H,00H,00H,00H,00H
DB 00H,00H,00H,80H,0C0H,0F0H,0BCH,18H
DB 00H,00H,00H,00H,0FCH,0FCH,08H,00H
DB 80H,80H,0C0H,60H,70H,60H,00H,00H,00H,00H,00H

DB 00H,00H,00H,00H,0C0H
DB 80H,00H,00H,00H,3FH,1FH,91H,0D1H
DB 91H,11H,11H,0D1H,91H,91H,0BFH,9FH
DB 80H,80H,80H,0C0H,0C0H,80H,00H,00H
DB 00H,00H,00H,00H,00H,00H,00H,08H
DB 08H,04H,03H,01H,0FFH,0FFH,01H,10H
DB 08H,08H,08H,84H,7FH,0FFH,0C2H,0C3H
DB 0C1H,0C1H,0C0H,0C0H,0C0H,0E0H,0FFH,60H
DB 00H,00H,00H

DB 00H,00H,00H,00H,0FFH
DB 0FFH,11H,11H,11H,11H,11H,0FFH,0FFH
DB 00H,00H,00H,0FFH,0FFH,10H,10H,10H
DB 10H,10H,10H,0FFH,0FFH,00H,00H,00H
DB 00H,00H,00H,00H,00H,00H,00H,00H
DB 10H,10H,10H,10H,11H,10H,10H,10H
DB 10H,10H,10H,0FFH,0FFH,12H,10H,10H
DB 10H,10H,10H,10H,10H,18H,1CH,18H,00H,00H,00H

DB 00H,00H,00H,00H,0FH
DB 07H,02H,02H,02H,02H,02H,07H,03H
DB 00H,00H,00H,07H,03H,01H,01H,01H
DB 01H,01H,01H,07H,03H,00H,00H,00H
DB 00H,00H,00H,00H,00H,00H,00H,00H
DB 00H,00H,00H,00H,00H,00H,00H,00H

DB 00H,00H,00H,0FH,07H,00H,00H,00H
DB 00H,00H,00H,00H,00H,00H,00H,00H,00H,00H

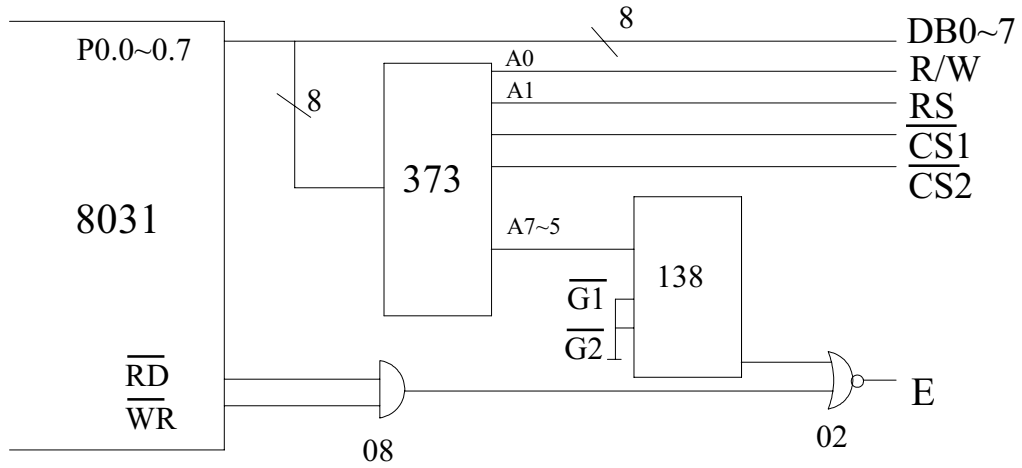
DB 00H,00H,00H,00H,00H
DB 00H,00H,00H,00H,00H,00H,00H,00H
DB 00H,00H,00H,00H,00H,00H,00H,00H
DB 00H,00H,00H,00H,00H,00H,00H,00H
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DB 00H,00H,00H,00H,00H,00H,00H,00H
DB 00H,00H,00H,00H,00H,00H,00H,00H
DB 00H,00H,00H,00H,00H,00H,00H,00H,00H,00H

DB 00H,00H,00H,60H,80H,81H
DB 81H,7FH,01H,00H,00H,81H,0FFH,81H
DB 00H,00H,0FFH,02H,1CH,20H,0FFH,00H
DB 3CH,42H,81H,0A1H,62H,0E7H,00H,00H
DB 0FFH,08H,08H,0FFH,00H,00H,7FH,80H
DB 80H,7FH,00H,0E0H,1CH,13H,13H,1CH
DB 0E0H,00H,00H,00H,00H,00H,00H,00H,00H,00H
DB 00H,00H,00H,00H,00H,00H,00H,00H

DB 00H,00H,00H,00H,00H
DB 00H,00H,00H,00H,00H,00H,00H,00H
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DB 00H,00H,00H,00H,00H,00H,00H,00H
DB 00H,00H,00H,00H,00H,00H,00H,00H
DB 00H,00H,00H,00H,00H,00H,00H,00H,00H,00H
END

;***** THE END OF PROGRAM (128*64) *****

● Application Circuit 1



● Application Circuit 2

